

EAST - [10.621246.wsp:1]

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L7: (1025) 365/191

L8: (4764) 365/189.05

L9: (4917) 365/233

L10: (15247) passgate or (pass adj gate) or (transmission adj gate)

L19: (160) (pipe adj latch) or pipelatch or pipe-latch

L21: (3) 10 and 19

L22: (27) 19 same memory

L28: (35938) pipilin\$4 or pipe-lin\$4 or (pipe adj lin\$4)

L33: (36) 10 and 28

L37: (922) 28 same memory

L39: (23) 37 and (odd near5 data)

L40: (1763) 365/189.02

L44: (34) 37 and 9

L41: (8) 37 and 40

L42: (2) 37 and 7

L43: (30) 37 and 8

L45: (5) (YOON near2 YOUNG-JIN).in.

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| 1 | <input type="checkbox"/> | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 5713005 A | 19980127 | 28 | Method and apparatus for pipelining data in an integrated circuit. | 713/600 | | | Proeb: |
| 2 | <input type="checkbox"/> | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 6094380 A | 20000725 | 14 | Memory device with a data output buffer and the control method therefor | 365/194 | 365/233 | | Kim, J |
| 3 | <input type="checkbox"/> | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 6192005 B1 | 20010220 | 20 | Clock control signal and output enable signal generator in semiconductor | 365/233 | 365/189.05; 365/194; 711/105 | | Lee, Y |
| 4 | <input type="checkbox"/> | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 6539454 B2 | 20030325 | 24 | Semiconductor memory synchronous pipeline | 711/105 | 365/233; 711/160 | | Mes, I |

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